University of Bahrain
College of IT
Department of CE

Computer Architecture (ITCE 321)
Academic Year: 2015-2016
Semester: I
Test 1

Prepared by Dr. Yasser Ismail **11-11-2015** **Time: 1 Hour**

Student I	
Student I	date
Section:	

Question	Points Attached
1 (43 marks)	40
2 (9 marks)	7
3 (15 marks)	13
(67 marks)	60

- No mobile
- Answer all questions.

YOU CAN ASSUME WHAT EVER YOU WANT!!

Q1

Answer the following questions:

1- The processor state of the MC68000 processor is: **(4 marks)**

PC<31..0> Program counter, only 24 bits is used of it.
IR <15..0> Instruction register with 16 bits.
D [7..0]<31..0> data registers (7 registers each 32 bits)
A [7..0]<31..0> address registers (7 registers each 32 bits)
Status <15..0> user and program status

4

2- Dhrystones is defined as: **(2 marks)**

a program used to measure performance of a computer.

1

3- The pre-fetching property of a processor means: **(2 marks)**

fetch the next instruction to be executed, before the previous one completes executing.
The instructions fetched are kept in a queue. So the limitation here is size of queue.

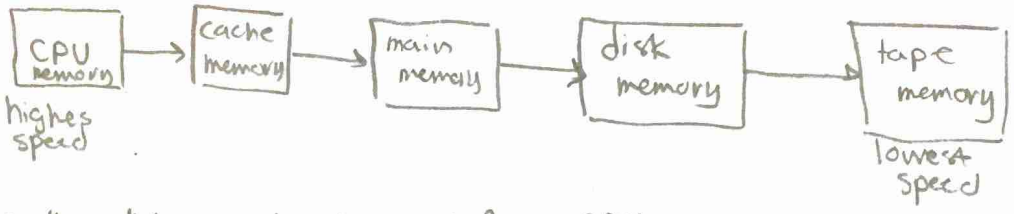
2

4- What is the meaning of the following RTN notations: **(5 marks)**

RTN	Meaning
;	The instructions (~~LHS/RHS~~) are executed in sequence. after the first complete, the next start.
:	The instructions on LHS and RHS can be executed at the same time.
←	assign value.
→	then (in condition)
<>	number of bits
@	duplication, Replecation
[]	index
#	Concatination
:=	naming – whats on RHS is description of LHS
()	to determine type (e.x sign) of arithmatic, or how short numbers are extended to longer (2's complement)

5

5- What is the hierarchy definition of data transfer? Give an example? **(2 marks)**



2

If the disk wants to read from CPU,
then the CPU makes its speed less to be compatible with the speed of disk memory
- The hierachy is useful to determine the speed and space.

6- Express the RTN of both interpretation and execution of an SRC instruction.
(3 marks)

- ¬run ∧ start ⟶ run ⟵ 1 — if it is not run and start then assign 1 to run
- run ⟶ IR ⟵ M[PC] : PC ⟵ PC + 4 — if it is run then put the content of the address of next instruction to be executed in instruction register IR and at the same time increment (PC) Program counter by 4.

3

7- Find the RTN and the corresponding addressing mode of each of the following instructions:
(12 marks)

12

	Instruction	RTN	Addressing Mode
1	ld r1, 32	R[r1] ⟵ M[32]	direct
2	ld r32, 25(r8)	R[r32] ⟵ M[25 + R[r8]]	displacement
3	st r3, 0(r7)	M[0+R[r7]] ⟵ R[r3]	displacement register indirect
4	la r8, 32	R[r8] ⟵ 32	immediate direct
5	ldr r13, -32	R[r13] ⟵ M[PC - 32]	relative
6	lar r8, 0	R[r8] ⟵ M[PC]	register relative

8- What are the components of the data path? **(2 marks)**

a. arithmatic
b. storage cells
c. their connections

2

9- Write the RTN of the following SRS instructions: **(6 marks)**

Instruction	RTN
Shra (:=op=27)	R[ra]<31..0> ← n@ R[rb]<31> # R[rb]<31..n>
shl (:=op=28)	R[ra]<31..0> ← R[rb]<31-n..0> # n@0
shc (:=op=29)	R[ra]<31..0> ← R[rb]<31-n..0> # R[rb]<31..32-n>

6

10- The main disadvantage of using brl over br instruction is: **(2 marks)**

brl will consume more area which means more power consumption, because it will store the content of PC register first in another register, then it will branch to the specified register in the instruction.

2

11- Given that IR<31..0> ← Mem[x]#Mem[x+1], then, the number of bits of each memory location is ---------16----------bits. **(3 marks)**

3

Q2:

Consider the following expression:

$$A = [Z - YM]^3$$

i. Evaluate the following expression using: **(6 marks)**

1. 4- address machine op / result / op1 / op2 / address of next instruction
2. Load/Store machine

st 9, r

Assuming that A, M, Y, Z are stored in the memory.

4- address machine	Load/Store machine

mpy A, Y, M, 105
sub A, A, Z, 209
mpy A, A, A, 313
mpy A, A, A, 417
	ld r1, Z
	ld r2, Y
	ld r3, M
	mpy r4, r2, r3
	sub r5, r1, r4
	mpy r5, r5, r5
	mpy r5, r5, r5
	st A, r5

memory location zero →

mpy A, Y, M, 13
1 3 3 3 3
= 13 byte
= low bit

6

ii. The memory access time of: **(3 mark)**

(4- address machine) = 9 × 4 = 36 times

mpy A, Y, M, —
1 2 3 4 5
9 8 7 6

(Load/Store machine) = (3×5) + 5 + (7×4) = 48 times
ld st mpy/sub

1 3 3 3 3
1 8

ld r1, 2
1 2 3
5 4
back to load back to take val

for load & store 5 times
for mpy, sub 7 times

mpy r1, r2, r3
1 2 3 4
7 6 5
back to store back to take value

st A, r5
1 2 3
5 4
back to store back to take val

5

Q3:

$ET = IC * CPI * \tau$

(instruction count, clock per instruction, tau width)

$f = \frac{1}{\tau}$, $\tau = \frac{1}{f}$

A) Consider the following machines: **(9 marks)**

1- Machine A: Avaerage CPI is = 4 cycles, Working frequency= 2Ghz
2- Machine B: Avarge CPI=3 cycles, Working frequency = 2.8 Ghz

If we execute a code that has 10000 instructions on both machines; calculate:

a- Execution time for machine A

$ET = IC * CPI * \tau = 1000 * 4 * \frac{1}{2 \times 10^9}$

$= 2 \times 10^{-6}$

b- Execution time for machine B

$ET = IC * CPI * \tau = 1000 * 3 * \frac{1}{2.8 \times 10^9}$

$= 1.07 \times 10^{-6}$

c- The speed up of B machine over A machine

$\text{Speed up} = \frac{max}{min} = \frac{2 \times 10^{-6}}{1.07 \times 10^{-6}} = 1.87$

$\text{Speed up percentage} = \frac{max - min}{min} * 100 = 86.92\ \%$

9

B) A digital computer has a memory unit with 32 bits word per location. The instruction set consists of 128 different operations. All instructions have an operations code part (opcode) and a memory address part. Each instruction is stored in one word of memory. **(6 marks)**

a. How many bits are needed for the opcode?

$\because 128 = 2^7$

$\therefore$ 7 bits are needed for the opcode

4

b. How many Bits are left for the address part of the instruction?

32 − 7 = 25 bits

c. What is the maximum allowable size for memory?

The maximum allowable size = 2^{32}

X